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10/550,741	09/22/2005	Radu Catalin Surdeanu	NL03 0347 US1	6084

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EXAMINER	
LIN, JOHN	

ART UNIT	PAPER NUMBER
2815	

NOTIFICATION DATE	DELIVERY MODE
12/11/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/550,741	SURDEANU ET AL.	
	Examiner	Art Unit	
	JOHN LIN	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-14 and 17-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-14 and 17-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 7, 10-14, 17 and 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,667,525, granted to "**Rhee**," in view of U.S. PGPUB 2001/0039107, granted to "**Suguro**," U.S. Patent 6,399,515, granted to "**Tao**."

Claims 6, 7 and 17: Rhee discloses an MIS type semiconductor device, Fig. 3, comprising:

a semiconductor substrate (21),

a gate electrode (23 and 24) formed on a gate insulating film (22) and formed of gate material,

wherein the gate electrode comprises:

a first layer of activated crystalline gate material (23) having a first side oriented towards the substrate and in contact with the gate insulating film, a second side oriented away from the substrate and a grain size, and

a second layer of gate material (24) in contact with the first layer of activated crystalline gate material at the second side of the first layer of activated crystalline gate material, the second layer of gate material having a grain size,

wherein the grain size of the first layer of activated crystalline gate material is smaller than the grain size of the second layer of gate material (column 5, lines 5-52).

Rhee appears not to explicitly disclose the grain size of the second layer of gate material is at least twice as large as the grain size of the first layer of activated crystalline gate material.

Suguro, however, discloses a gate electrode with a second layer (3') having a grain size at least twice as large as the grain size of a first layer (3) to reduce the variations in threshold voltage (Fig. 3; paragraphs [0081]-[0096]).

To reduce the variations in threshold voltage therefore it would have been obvious to modify Rhee to have made the grain size of the second layer of gate material is at least twice as large as the grain size of the first layer of activated crystalline gate material.

Rhee also appears not to explicitly disclose the first layer of activated crystalline gate material having a doping level of 10^{19} ions/cm^3 (claim 6), 10^{20} ions/cm^3 (claim 7), $5x10^{20}$ ions/cm^3 (claim 17) or higher.

Tao, however, discloses and motivates a gate electrode doped to a level greater than about 10^{20} dopant atoms per cubic centimeter in order to assure optimal conductivity (column 9, lines 14-37).

To assure optimal conductivity therefore it would have been obvious to modify Rhee so the first layer of activated crystalline gate material has a doping level greater than 10^{19} ions/cm^3. In the case where the claimed ranges overlap or lie inside ranges disclosed by the prior art a *prima facie* case of obviousness exists (M.P.E.P. § 2144.05).

Claim 10: Rhee discloses the second layer of gate material consists of polycrystalline gate material (column 5, lines 5-10).

Claim 11: Suguro discloses the grain size of the second layer is more than 30 nm (paragraph [0094]). In the case where the claimed ranges overlap or lie inside ranges disclosed by the prior art a *prima facie* case of obviousness exists (M.P.E.P. § 2144.05). It would therefore have been obvious to have made the grain size in the second layer below about 40 nm.

Claims 12, 20 and 21: Suguro discloses the first layer is crystalline and has grains below 10 nm. In the case where the claimed ranges overlap or lie inside ranges disclosed by the prior art a *prima facie* case of obviousness exists (M.P.E.P. § 2144.05). It would therefore have been obvious to have made the first layer have grains below 5 nm. Suguro also discloses the grain size in the second layer is below about 30 nm (paragraph [0094]). Suguro therefore disclose the grain size of the second layer of gate material is about six times as large as the grain size of the first layer of activated crystalline gate material.

Claim 13: Rhee discloses a gate insulator (22) is provided between the semiconductor substrate and the gate electrode (Fig. 3; column 5, lines 26-27).

Claim 14: Gardner et al. teach the device is a transistor (column 5, lines 5-6).

Claim 22: The recitation "the grain size of the first layer of activated crystalline gate material reduces gaps between the first layer of activated crystalline gate material and the gate insulating film" has been considered and determined to be functional language, making the claim scope not distinguish over a layer of activated crystalline

gate material capable of having grain size to reduce gaps between a layer of activated crystalline gate material and a gate insulting film. The claim recitations do not require the grain size of the first layer of activated crystalline gate material reduces gaps between the first layer of activated crystalline gate material and the gate insulating film to be part of the elements limiting the claim scope. See MPEP § 2114, and precedents cited therein.

Claim 23: Rhee discloses the first layer of activated crystalline gate material is silicon (column 5, lines 5-10).

Claim 24: Rhee discloses an MIS type semiconductor device, Fig. 3, comprising:

a semiconductor substrate (21);

a gate insulating film (22); and

a gate electrode (23 and 24) formed on the gate insulating film, the gate electrode including:

a first layer of activated crystalline gate material (23) having a first side oriented towards the substrate and in contact with the gate insulating film, a second side oriented away from the substrate and a grain size of less than about 5 nm, and

a second layer of gate material (24) in contact with the first layer of activated crystalline gate material at the second side of the first layer of activated crystalline gate material, the second layer of gate material having a grain size of less than about 40 nm,

wherein the grain size of the first layer of activated crystalline gate material is smaller than the grain size of the second layer of gate material (column 5, lines 5-52).

Rhee appears not to explicitly disclose the first layer of activated crystalline gate material has a grain size of less than about 5 nm and the second layer of gate material has a grain size of less than about 40 nm.

Suguro, however, discloses a gate electrode with a first layer (3) with a grain size of 10 nm or less and a second layer (3') having a grain size of more than 30nm to reduce the variations in threshold voltage (Fig. 3; paragraphs [0081]-[0096]).

To reduce the variations in threshold voltage therefore it would have been obvious to modify Rhee to have made the first layer of activated crystalline gate material have a grain size of less than about 5 nm and the second layer of gate material have a grain size of less than about 40 nm. In the case where the claimed ranges overlap or lie inside ranges disclosed by the prior art a *prima facie* case of obviousness exists (M.P.E.P. § 2144.05).

Rhee also appears not to explicitly disclose the first layer of activated crystalline gate material having a doping level of 10^{19} ions/cm^3.

Tao, however, discloses and motivates a gate electrode doped to a level greater than about 10^{20} dopant atoms per cubic centimeter in order to assure optimal conductivity (column 9, lines 14-37).

To assure optimal conductivity therefore it would have been obvious to modify Rhee so the first layer of activated crystalline gate material has a doping level greater

than 10^{19} ions/cm^3. In the case where the claimed ranges overlap or lie inside ranges disclosed by the prior art a *prima facie* case of obviousness exists (M.P.E.P. § 2144.05).

Claims 8, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee in view of Suguro in view of Tao as applied to claims 6, 7, 10-14, 17 and 20-24 above, and further in view of U.S. Patent 6,222,251, granted to "**Holloway**."

Claims 8, 18 and 19: Rhee in view of Tao discloses all the limitations of claim of claim 6. Rhee in view of Tao appears not to explicitly disclose the doping implant in the activated gate material has an abruptness of about 2nm or more (claim 8); about 1.5nm (claim 18) or more; or about 1nm (claim 19).

Holloway discloses the doping profile across a gate electrode is a resulting-affecting parameter. Holloway discloses having a doping profile across a gate electrode from an upper surface to a gate oxide boundary affects the depletion region of the gate (column 5, line 30—column 6, line 8) and further discloses that different applications desires different depletion regions (column 1, line 56 – column 2, line 3).

Since Holloway discloses the doping profile across a gate electrode is a result-affecting parameter, therefore it would have been obvious to optimize the doping profile of a gate, such as the abruptness of the doping profile (see M.P.E.P. § 2144.05).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee in view of Suguro in view of Tao as applied to claims 6, 7, 10-14, 17 and 20-24 above, and further in view of U.S. Patent 6,160,300, granted to "**Gardner**."

Claim 9: Rhee in view of Tao discloses all the limitations of claim of claim 6 and Rhee further discloses the second layer of gate material consists of polycrystalline gate material (column 5, lines 5-10). Rhee in view of Tao appears not to explicitly disclose the second layer of gate material consists of amorphous gate material.

Gardner, however, discloses polysilicon and amorphous silicon are suitable materials for an upper layer of a gate electrode (column 7, lines 21-32). The selection of a known material based on its suitability for its intended purpose is obvious (see, for example, MPEP § 2144.07, and precedents cited therein).

Because polysilicon and amorphous silicon are art-recognized suitable materials for an upper layer of a gate electrode, therefore, it would have been obvious to modify Rhee to have made the second layer of gate material from amorphous gate material.

Response to Arguments

Applicant's arguments filed November 11, 2009 have been fully considered but they are not persuasive.

Applicant contends Rhee and Suguro are directed to different types of devices that use different types of gate materials, and the combination would involve extensively modifying cited disclosures of Rhee and Suguro.

Examiner notes that Suguro is not relied up for the disclosure of the materials of the gate. Suguro is relied upon for the grain sizes of the gate. Rhee discloses a gate structure with a lower layer 23 having grain sizes smaller than an upper layer 24 (column 5, lines 5-10), but does not disclose how much smaller they are. Rhee and

Suguro are not different devices, they are both MOS devices and therefore are analogous art.

Applicant, referring to M.P.E.P. § 2141, states, "the elements in combination do not merely perform the function that each element performs separately."

Examiner notes that Rhee and Suguro are analogous art because they are both MOS devices. Since Rhee discloses a gate structure with a lower layer 23 having grain sizes smaller than an upper layer 24 (column 5, lines 5-10) and Suguro discloses a gate electrode with a lower layer 3 having a grain sizes of 30 nm or less and an upper layer 3' having grain size of more than 30 nm to reduce the variations of threshold voltage, one of ordinary skill in the art would modify Rhee to have the lower layer have a grain size of 30 nm or less and the upper layer have a grain size of more than 30 nm. Rhee in view of Suguro therefore disclose the grain size of the second layer of gate material is at least twice as large as the grain size of the first layer of activated crystalline gate material.

Applicant contends the proposed combination appears to be improperly based on applicant's disclosure in a hindsight reconstruction of the claimed invention.

Examiner notes that it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Applicant contends Rhee does not teach that lower poly-SiGe is activated crystalline material.

Examiner notes that Rhee discloses lower poly-SiGe is activated crystalline material (column 6, lines 23-29 and 48-52).

Applicant contends Gardner teaches away from the proposed § 103(a) rejection because replacing layer 24 of Rhee with amorphous silicon would render Rhee unsatisfactory for restraining the diffusion of Ge through the grain boundary.

Examiner notes that Gardner is relied upon for the teaching of the material of the gate. Rhee in view of Gardner as applied to claim 9, would disclose the second layer of ate material consists of amorphous gate material having a grain size smaller than the first layer.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN LIN whose telephone number is (571)270-1274. The examiner can normally be reached on M-F, 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matthew E Warren/
Primary Examiner, Art Unit 2815

/J. L./
Examiner, Art Unit 2815